

Abstract of the Disclosure

5 A clock recovery circuit includes a delay locked loop, and a clock phase
interpolator circuit. The delay locked loop provides multiple phases of an input
clock signal to the interpolator circuit, which interpolates between two of the clock
phases to provide a clock signal at a desired phase. The clock phase interpolator
circuit includes selectable differential transistor pairs coupled to variable current
sources. Different differential transistor pairs are driven by clock signals of different
phases provided by the delay locked loop circuit. Two differential transistor pairs
10 are selected, and currents provided to the selected differential transistor pairs are
adjusted to provide an output clock of the desired phase.

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